CLAIMS

What is claimed is:

1. A system comprising:

a processor; and

at least one synchronous random access memory (SRAM) device comprising:

a plurality of memory array blocks each configured to store data;

a write driver located locally with respect to the plurality of memory array blocks and configured to receive data on an input line and to drive the data into one or more of the plurality of memory array blocks on one or more data lines coupled between the write driver and the plurality of memory array blocks; and

at least one logical device configured to provide a block select signal to each of the plurality of memory array blocks such that each of the plurality of memory array blocks may receive data from the write driver simultaneously.

2. The system, as set forth in claim 1, wherein the write driver comprises a plurality of write drivers, each of the plurality of write drivers corresponding to one of the plurality of memory array blocks and each of the plurality of write drivers having a corresponding data line coupled between the write driver and the corresponding memory array block, wherein the data line provides a path on which to drive the data from the write driver into the corresponding memory array block.

3. The system, as set forth in claim 1, wherein at least one logical device is configured to receive one or more block select signals, the block select signal corresponding to a memory array block and wherein enabling the block select signal provides write access to the corresponding memory array block.

4. The system, as set forth in claim 3, wherein the one or more logical devices are configured to receive a testmode signal wherein enabling the testmode signal provides write access to each of the plurality of memory array blocks simultaneously.

5. The system, as set forth in claim 4, wherein the testmode signal is enabled during burn-in testing of the SRAM device.

6. The system, as set forth in claim 4, wherein the at least one logical device comprises one or more NAND gates, each NAND gate corresponding to one of the plurality of memory array blocks and configured to receive a block select signal and a testmode signal.

7. A memory device comprising:

a plurality of memory array blocks each configured to store data;

a write driver located locally with respect to the plurality of memory array blocks and configured to receive data on an input line and to drive the data into the plurality of memory array blocks on data lines coupled between the write driver and the plurality of memory array blocks; and

at least one logical device configured to provide a block select signal to each of the plurality of memory array blocks such that each of the plurality of memory array blocks may receive data from the write driver simultaneously.

8. The memory device, as set forth in claim 7, wherein the write driver comprises a plurality of write drivers, each of the plurality of write drivers corresponding

to one of the plurality of memory array blocks and each of the plurality of write drivers having a corresponding data line coupled between the write driver and the corresponding memory array block, wherein the data line provides a path on which to drive the data from the write driver into the corresponding memory array block.

9. The memory device, as set forth in claim 7, wherein the at least one logical device is configured to receive one or more block select signals, the block select signal corresponding to a memory array block and wherein enabling the block select signal provides write access to the corresponding memory array block.

10. The memory device, as set forth in claim 9, wherein the at least one logical device is configured to receive a testmode signal wherein enabling the testmode signal provides write access to each of the plurality of memory array blocks simultaneously.

11. The memory device, as set forth in claim 10, wherein the testmode signal is enabled during burn-in testing of the memory device.

12. The memory device, as set forth in claim 10, wherein the at least one logical device comprises one or more NAND gates, each NAND gate corresponding to

one of the plurality of memory array blocks and configured to receive a block select signal and a testmode signal.

13. The memory device, as set forth in claim 7, wherein the memory device comprises a synchronous random access memory (SRAM) device.

14. A method of simultaneously accessing a plurality of memory array blocks in a synchronous random access memory (SRAM) device, comprising the acts of:

receiving a first signal at a first input of a logical device, the first signal corresponding to a memory array block selection signal;

receiving a second signal at a second input of the logical device, the second signal corresponding to a testmode enable signal;

producing an output signal from the logical device, wherein the output signal corresponds to one of the first signal and the second signal;

enabling a plurality of memory array block select lines in response to the output signal from the logical device; and

writing data to a plurality of memory array blocks corresponding to the enabled memory array block select lines.

15. The method of simultaneously accessing a plurality of memory array blocks in a synchronous random access memory (SRAM) device, as set forth in claim 14, wherein the acts of receiving comprise receiving the first signal and the second signal at a NAND gate.

16. The method of simultaneously accessing a plurality of memory array blocks in a synchronous random access memory (SRAM) device, as set forth in claim 14, comprising:

producing an output signal from the logical device, wherein the output signal corresponds to the testmode enable signal;

enabling a plurality of memory array block select lines in response to the output signal, each of the plurality of memory array block select lines corresponding to one of a plurality of memory array blocks; and

writing data to the plurality of memory array blocks.

17. A method of manufacturing a memory device, comprising the acts of:

providing a plurality of memory array blocks each configured to store data;

providing a write driver located locally with respect to the plurality of memory array blocks and configured to receive data on an input line and to drive the data into the plurality of memory array blocks on data lines coupled between the write driver and the plurality of memory array blocks; and

providing at least one logical device configured to provide a block select signal to each of the plurality of memory array blocks such that each of the plurality of memory array blocks may receive data from the write driver simultaneously.

18. The method of manufacturing a memory device, as set forth in claim 17, wherein the act of providing a write driver comprises the act of providing a plurality of write drivers, each of the plurality of write drivers corresponding to one of the plurality of memory array blocks and each of the plurality of write drivers having a corresponding data line coupled between the write driver and the corresponding memory array block, wherein the data line provides a path on which to drive the data from the write driver into the corresponding memory array block.

19. The method of manufacturing a memory device, as set forth in claim 17, wherein the act of providing at least one logical device comprises the act of providing one or more logical devices which are configured to receive one or more block select signals, the block select signal corresponding to a memory array block and wherein enabling the block select signal provides write access to the corresponding memory array block.

20. The method of manufacturing a memory device, as set forth in claim 19, comprising the act of configuring at least one logical device to receive a testmode signal wherein enabling the testmode signal provides write access to each of the plurality of memory array blocks simultaneously.

21. The method of manufacturing the memory device, as set forth in claim 20, wherein the act of providing at least one logical device comprises the act of providing one or more NAND gates, each NAND gate corresponding to one of the plurality of memory array blocks and configured to receive a block select signal and a testmode signal.